



FIG.1

212	214	216	218	210
NO. of active lines (M)	Division ratio (R)	No. of reference clocks per scanning period (N)	Frame frequency	
220	160	1 222	18 224	69.4 Hz 226
	130	1	22	69.9 Hz
230	100	1 232	28	71.4 Hz
	70	2 232	20 234	71.4 Hz 236
	40	4	18	69.4 Hz
	10	16	18	69.4 Hz
240	160	1	21	59.5 Hz
	130	1	26	59.2 Hz
	100	1 242	33 244	60.6 Hz
	70	2 242	24 244	59.5 Hz 246
	40	4	21	59.5 Hz
	10	16	21	59.5 Hz

FIG.3

Signal name	Meaning	"Low"	"High"
CS	chip select	accessible	inaccessible
RS	register address/data selection	address	data
E	data write/read activation	active	inactive
RW	data write/read selection	write	read
D	interactive data	—	—



FIG.2

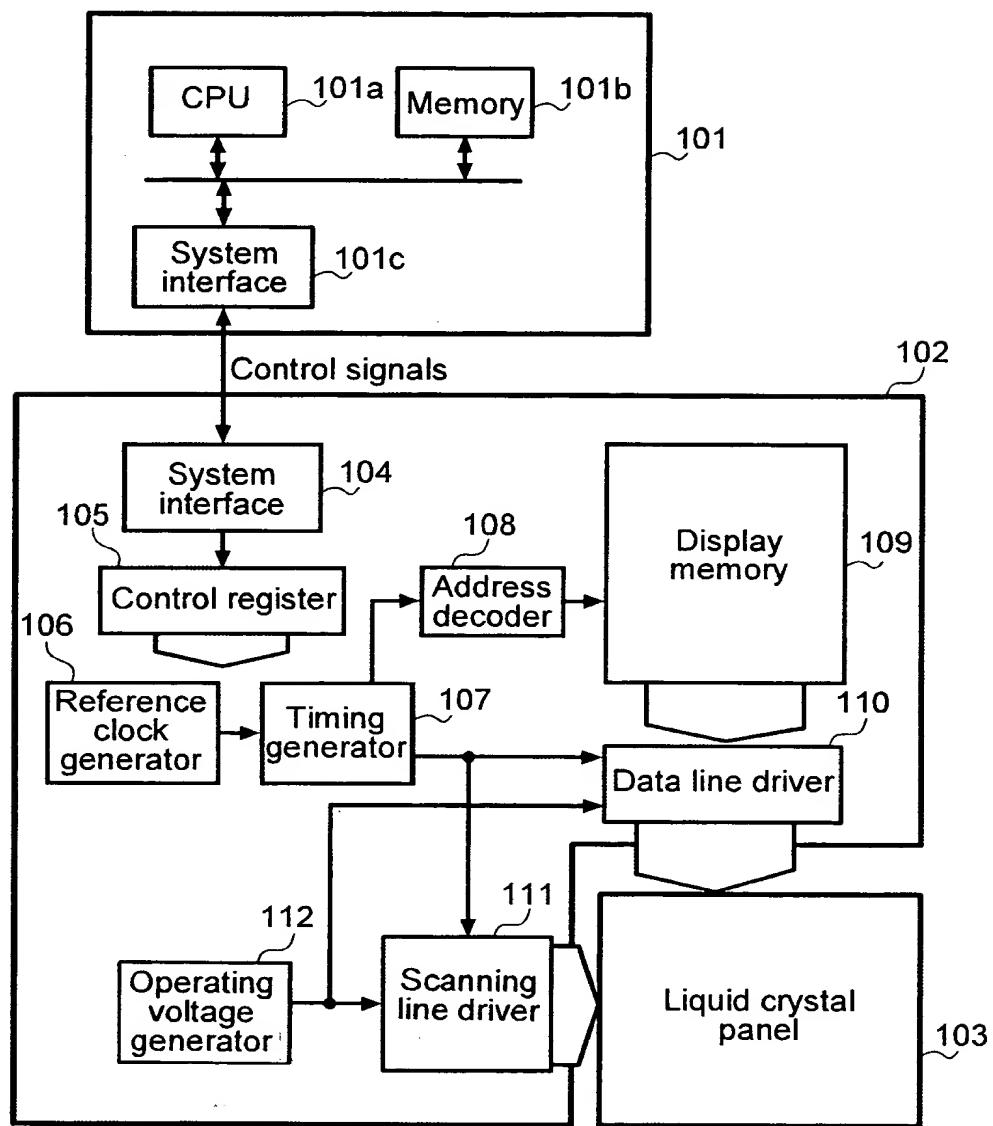




FIG.4

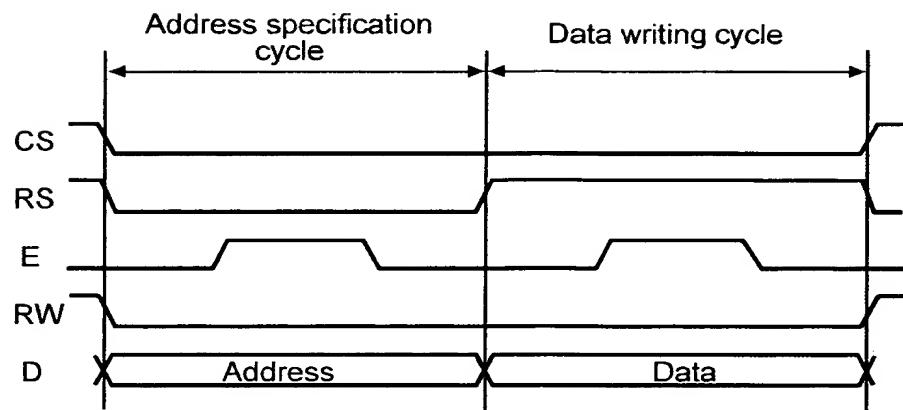


FIG.5

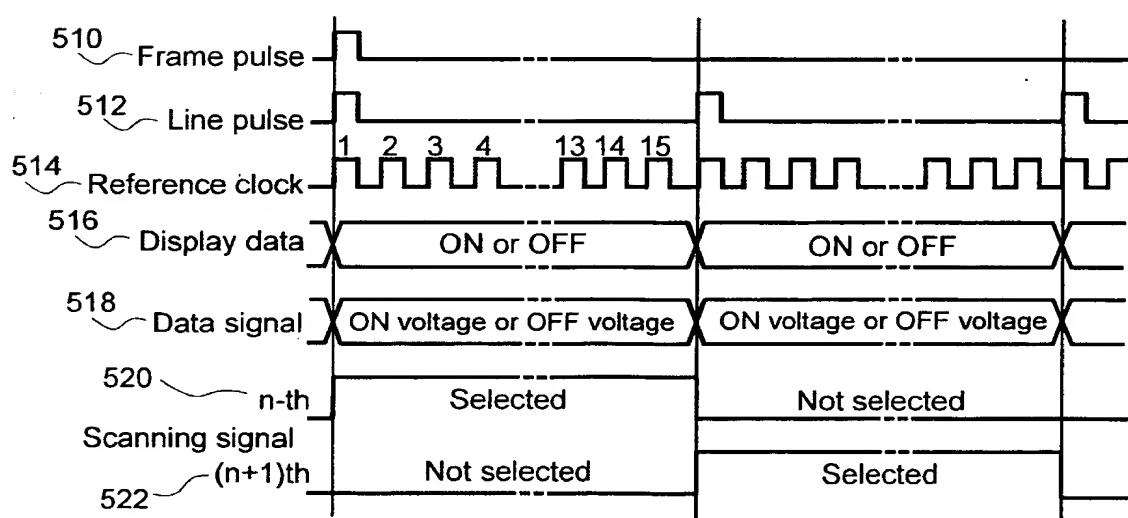




FIG.6

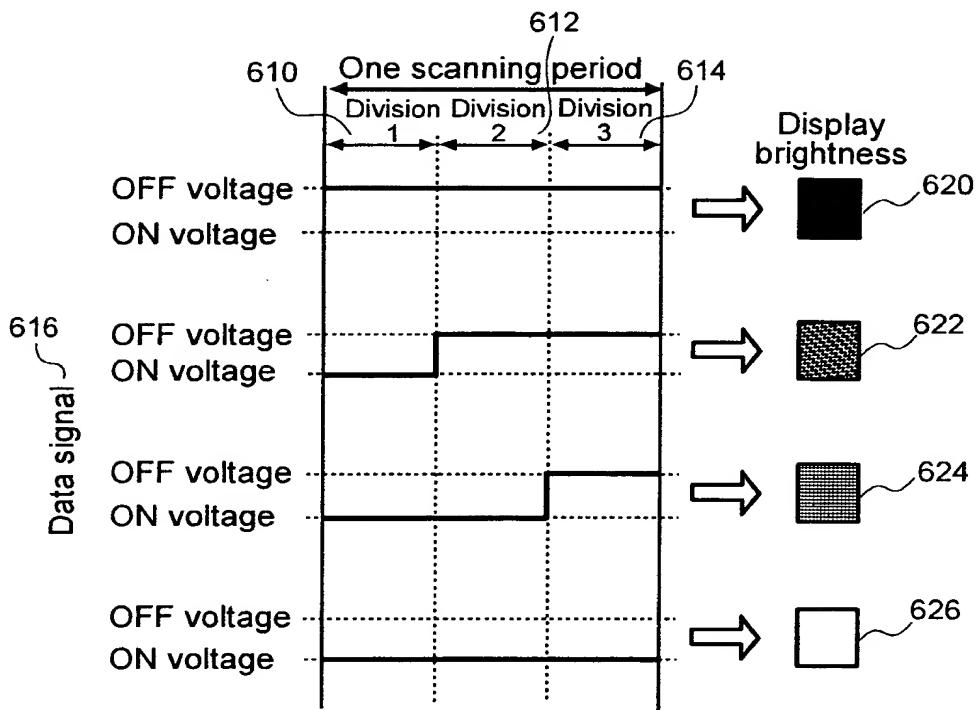




FIG.7

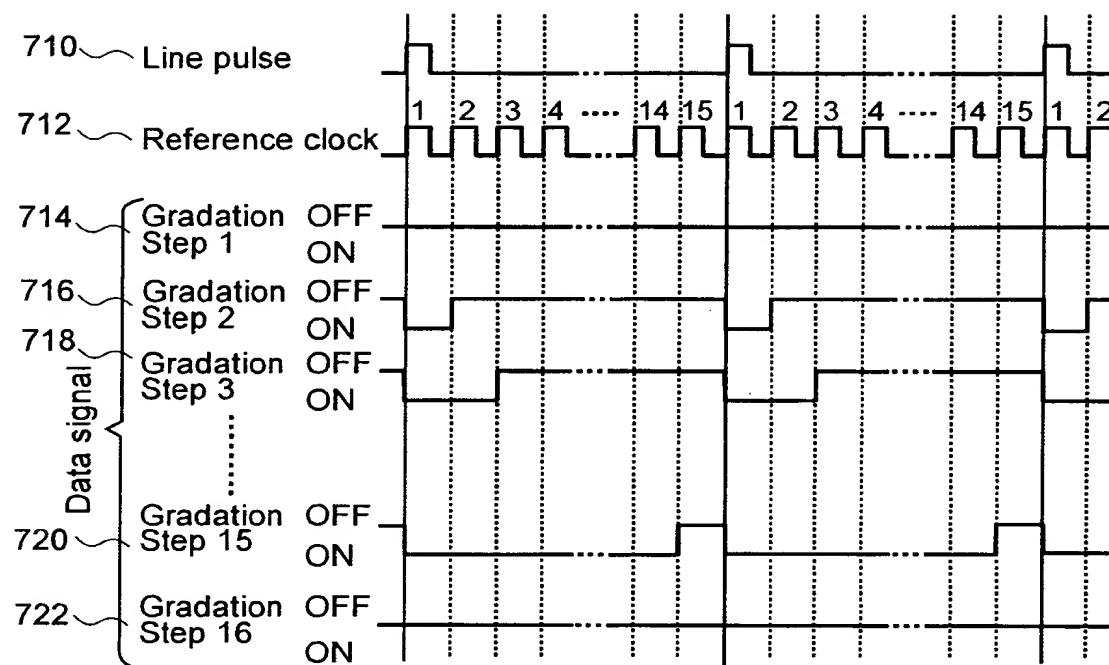




FIG.8

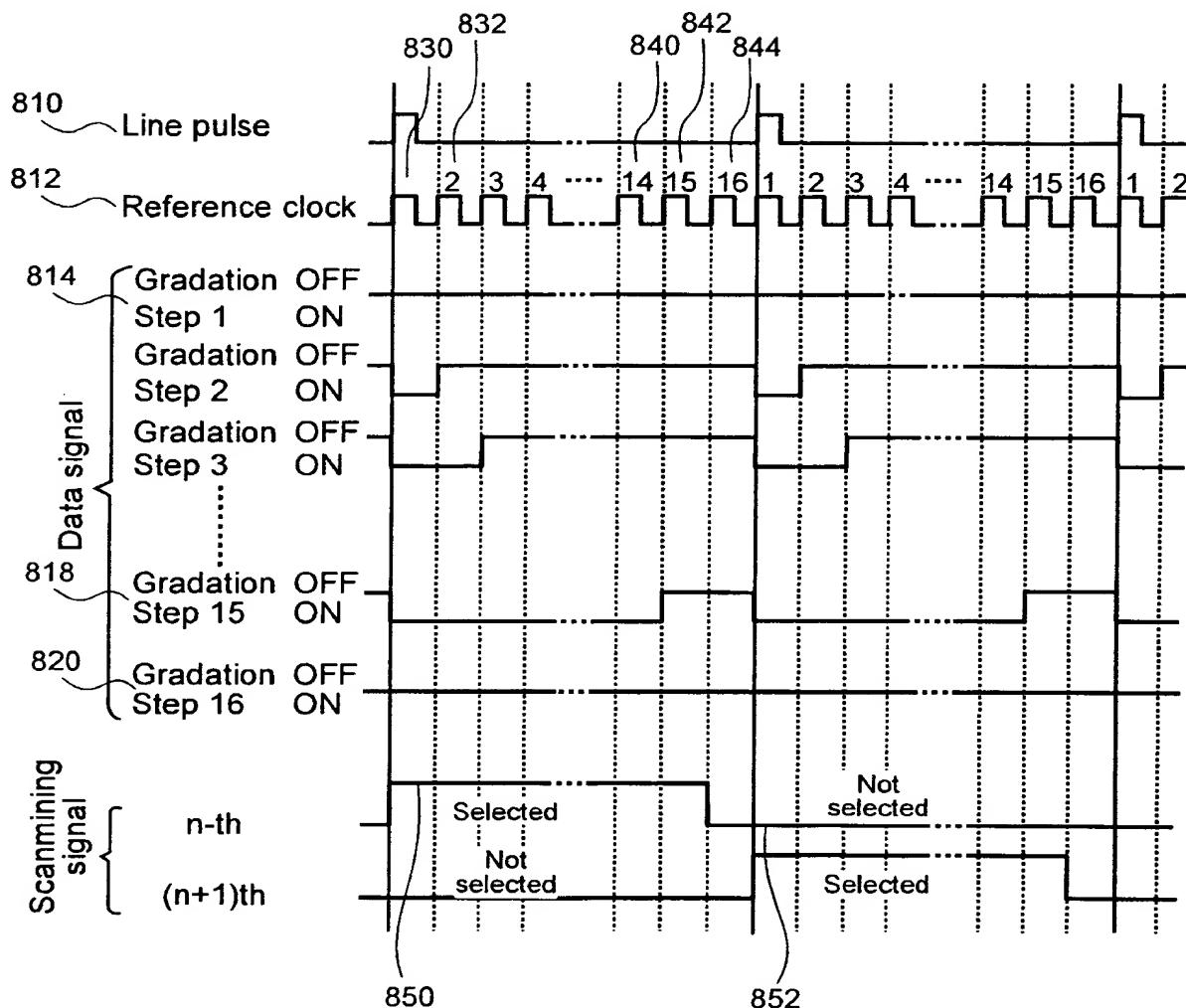




FIG.9

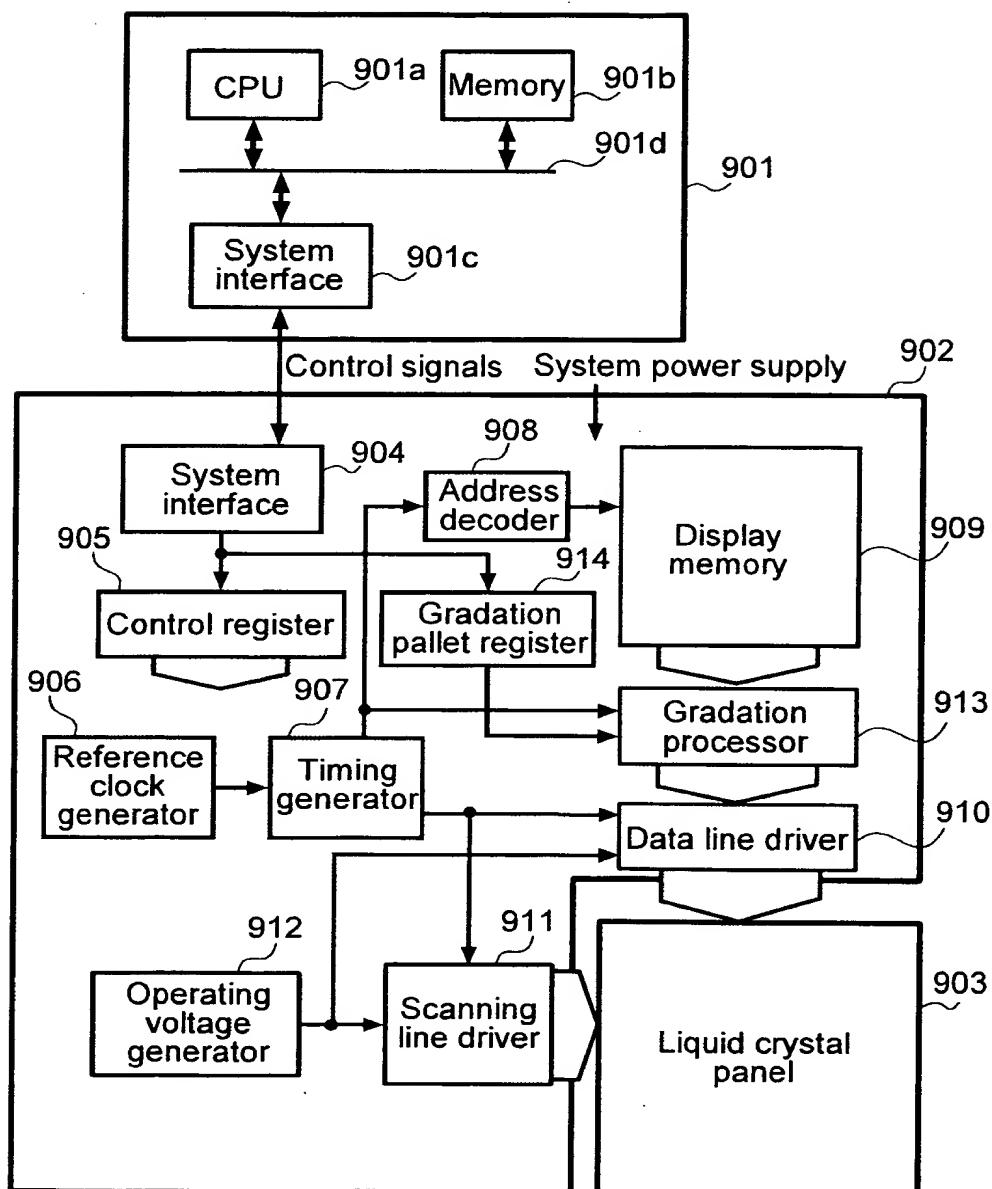




FIG.10

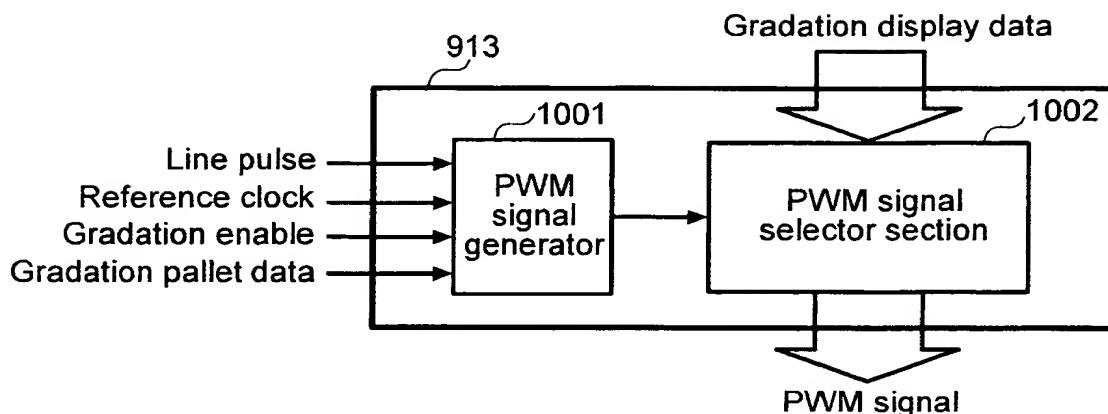


FIG.11

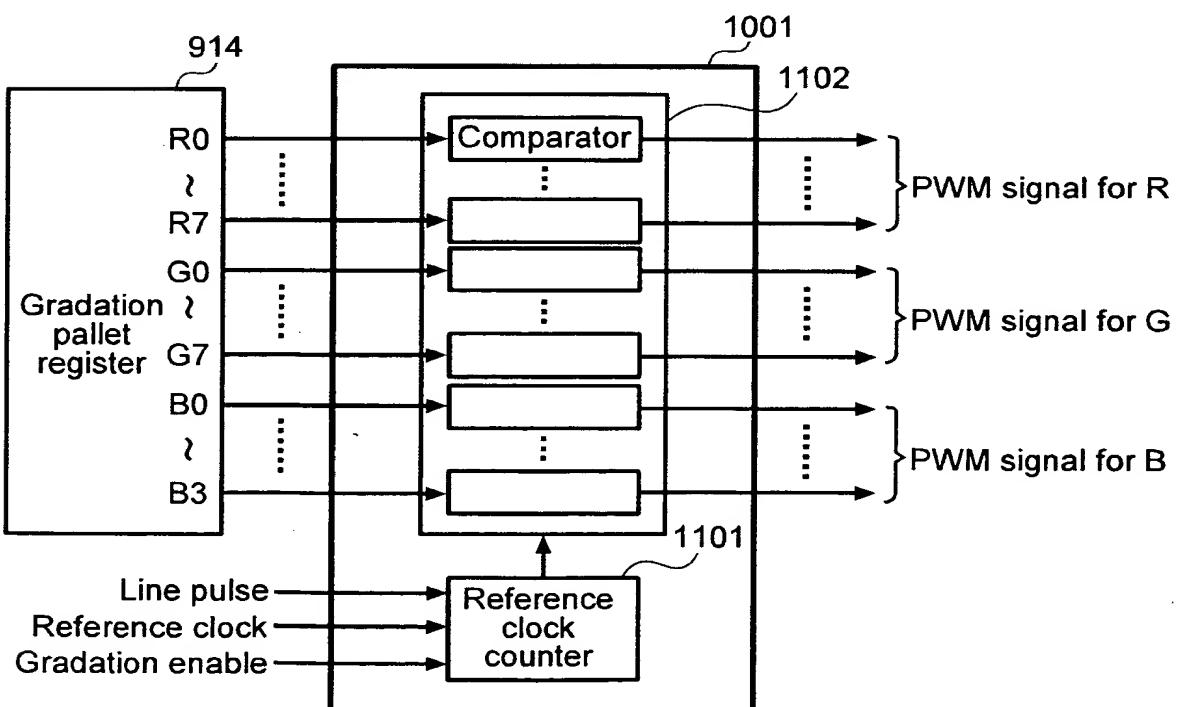




FIG.12

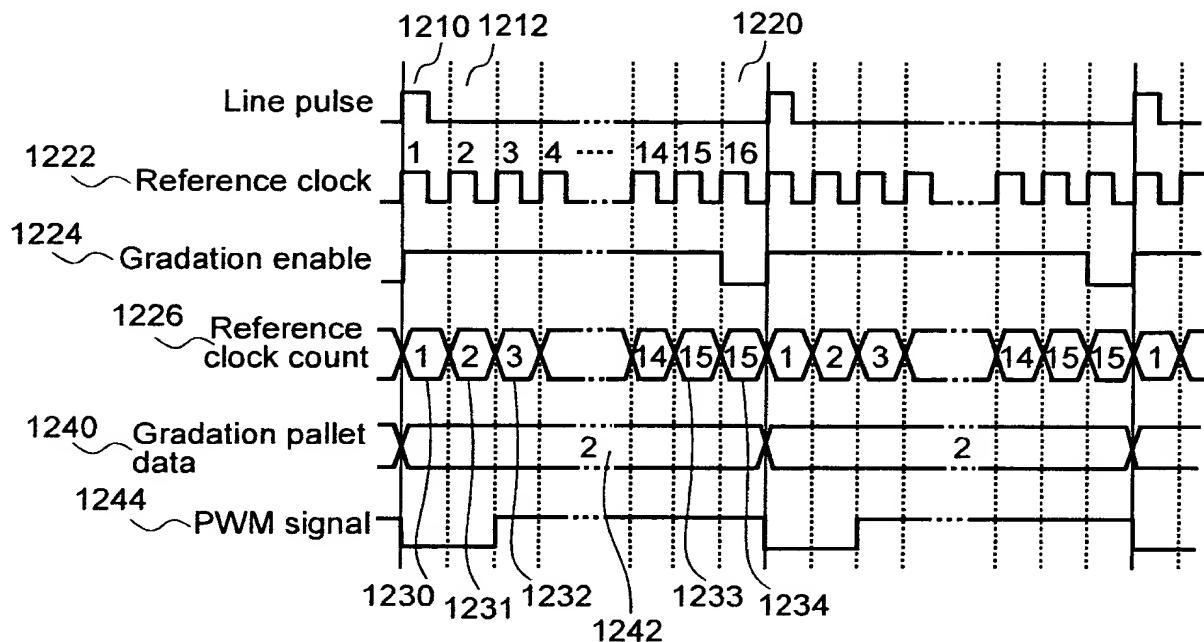


FIG.13

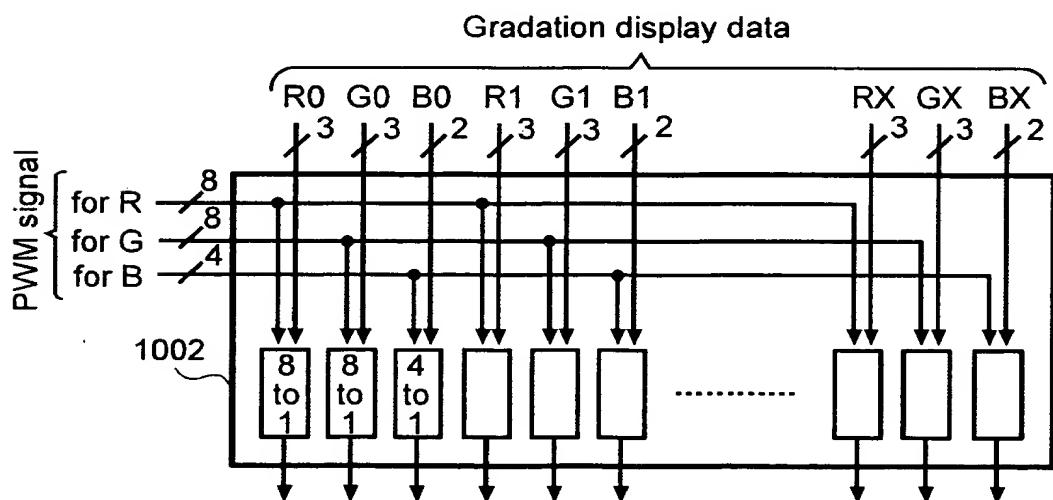




FIG.14

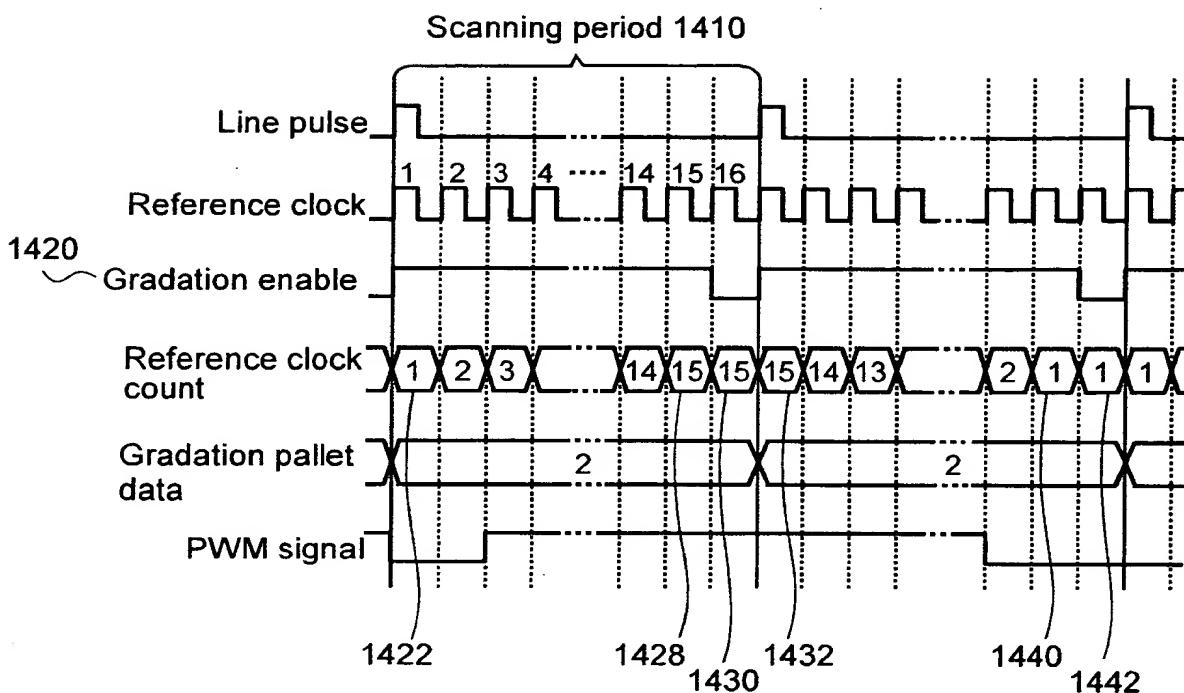




FIG.15a

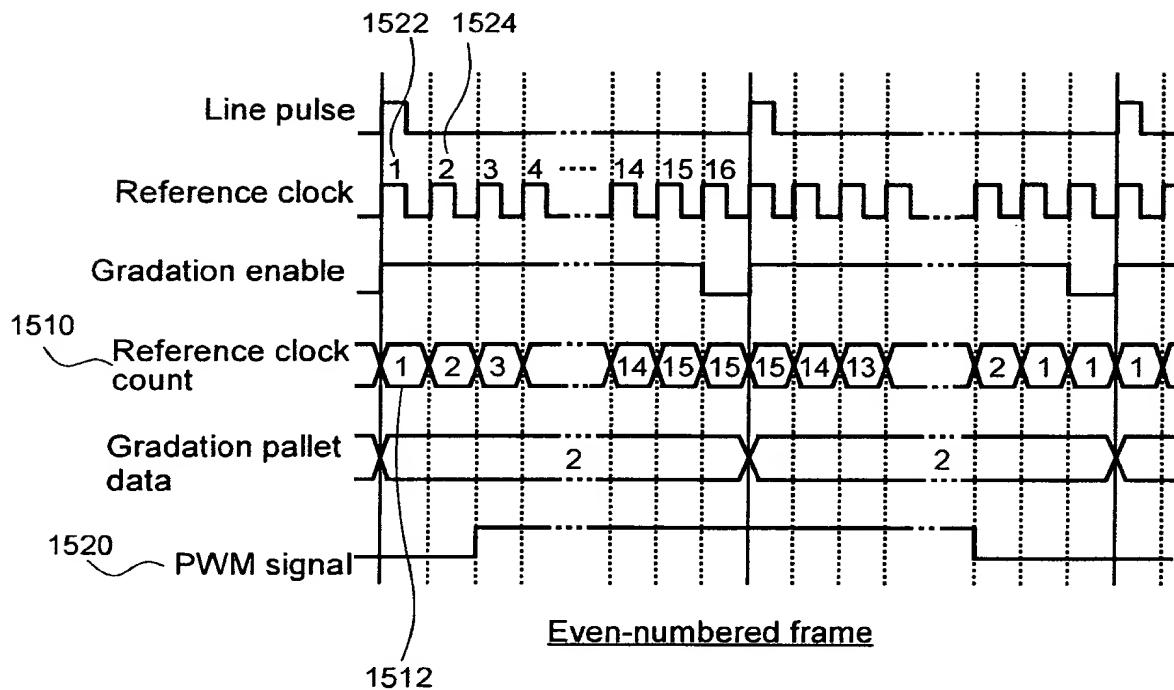




FIG.15b

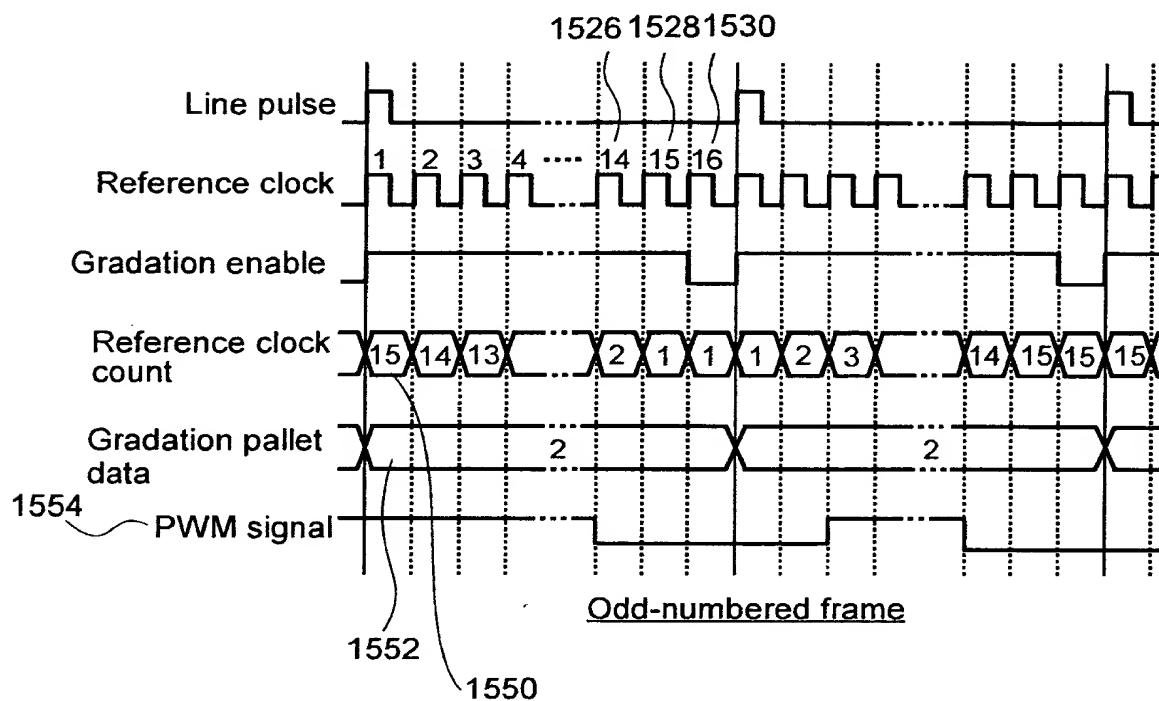




FIG.16

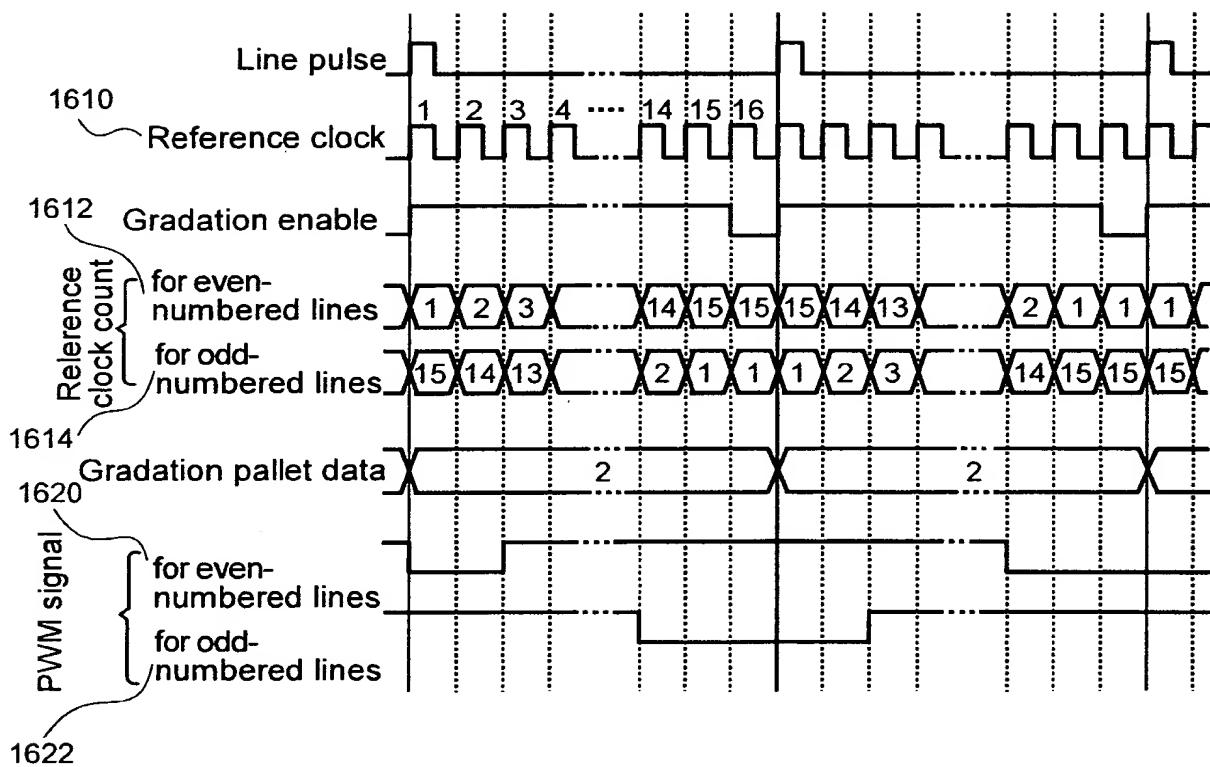




FIG.17

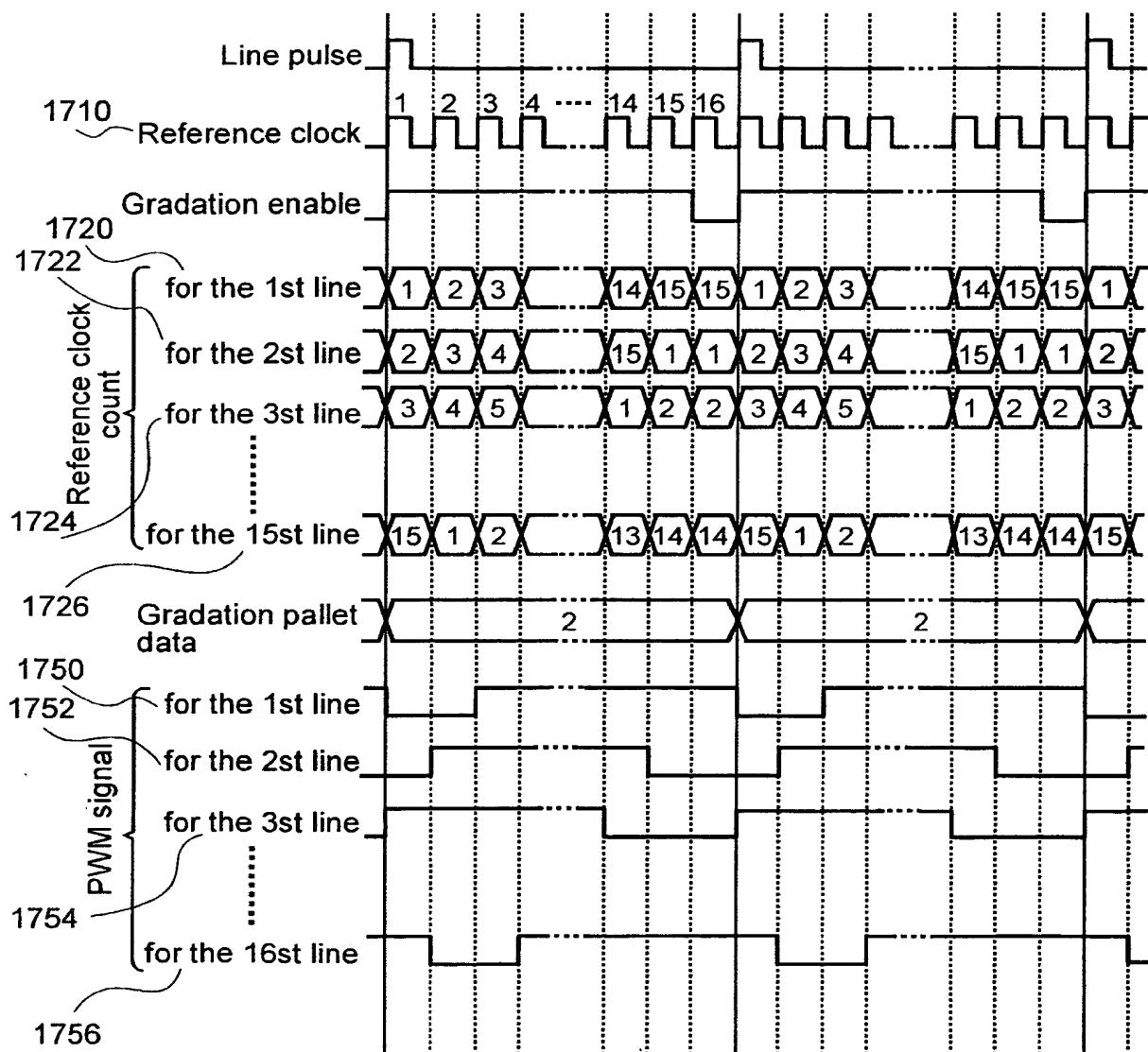




FIG.18a

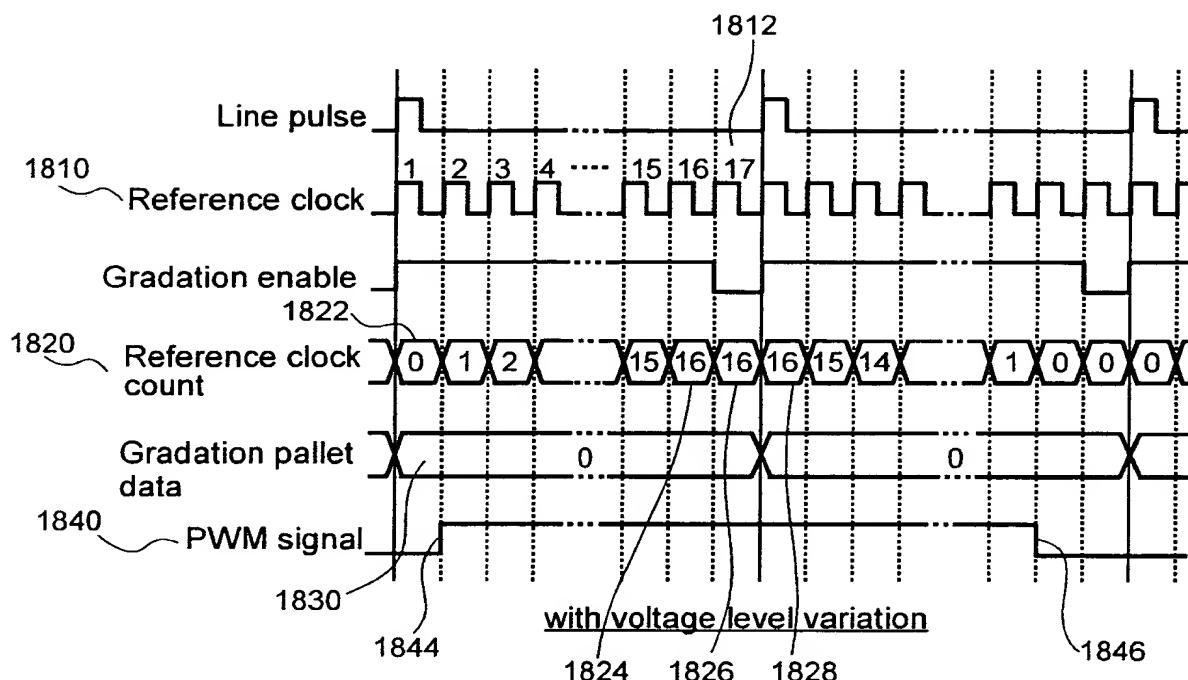
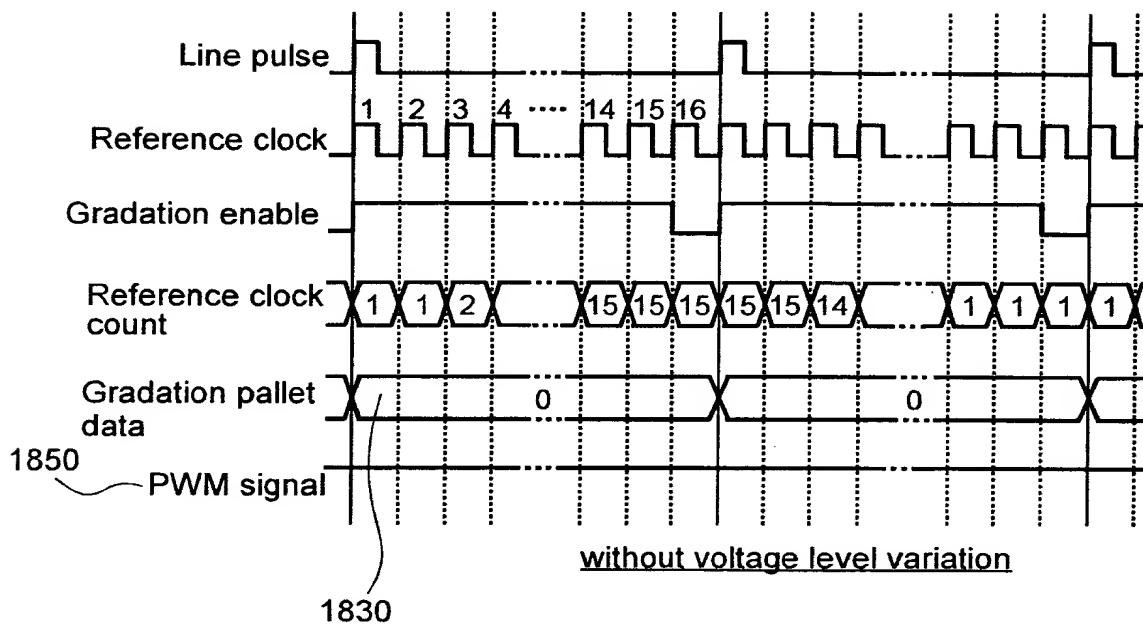




FIG.18b





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Title: Liquid Crystal Display Controller
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FIG.19

